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IN THE CLAIMS

--1. (Amended) A semiconductor device [having] comprising:

at least three [or more] power terminals [superimposed on each other,] provided one above the other; and

at least one semiconductor chip [is connected electrically in a way to be sandwiched] having an upper surface and a lower surface and interposed between a predetermined two power terminals [among said power terminals, in a semiconductor device for large power] of said at least three power terminals with the upper and lower surfaces of the at least one semiconductor chip electrically connected to the two power terminals.

2. (Amended) The semiconductor device according to claim 1, wherein [a power terminal on one end among said superposed power terminals and a power terminal on the other end among said superposed power terminals are led out] the uppermost one and lowermost one of said at least three power terminals extend in the same direction.

3. (Amended) The semiconductor device according to claim 2, wherein a power terminal positioned at the middle among said [superposed power terminals is led out] at least three power terminals extends in a direction opposite to or perpendicular to [a power terminal on said one or other end] the uppermost one or lowermost one of said at least three power terminals.

4. (Amended) The semiconductor device according to claim 1, wherein one face of said at least one semiconductor chip [sandwiched] interposed between said two power terminals is connected to one power terminal of said two power terminals by soldering or pressure welding, and [the other] another face is connected to [the other] another power terminal of said two power terminals by soldering or pressure welding through a buffer plate.

5. (Amended) The semiconductor device according to claim 1, wherein two currents flow in opposite directions in said uppermost one and lowermost one of said at least three power terminals, while said at least one semiconductor chip [operates, so that the current flows in the opposite direction for the power terminal on one end among said superposed power terminals and for the power terminal on the other end] is operating.

6. (Amended) The semiconductor device according to claim 1, wherein said at least one semiconductor chip [sandwiched] interposed between said two power terminals [is made of] includes a plurality of semiconductor chips, and [an] at least one insulation layer is provided [among] between said plurality of semiconductor chips.

7. (Amended) The semiconductor device according to claim 6, wherein said plurality of semiconductor chips [comprises] includes at least one transistor and at least one diode, and [a] wherein at least one control electrode is connected to said at least one transistor to control said at least one transistor.

8. (Amended) The semiconductor device according to claim 7, wherein said at least one transistor has a control electrode [and a] pad, said control electrode is connected to said control electrode pad [of said transistor are connected] by wire bonding[, or connected directly by sandwiching a buffer plate] or by interposing a buffer plate between said control electrode and said control electrode pad.

9. (Amended) The semiconductor device according to claim 7, wherein said control electrode is led out in a direction opposite to or perpendicular to [a power terminal positioned on one end of said power terminal or on the other end of said power terminal] the uppermost one or lowermost one of said at least three power terminals.

10. (Amended) The semiconductor device according to claim 4, wherein the [power terminals positioned on one end of said power terminal and the power terminal on the other end] uppermost one and lowermost one of said at least three power terminals have a screw fixing structure so as to connect said at least one semiconductor [chips] chip by pressure welding between [any] said two power terminals [of said power terminals superimposed on each other].

Claims 11-19 (New).--